Strain-Gated Piezotronic Transistors Based on Vertical Zinc Oxide Nanowires

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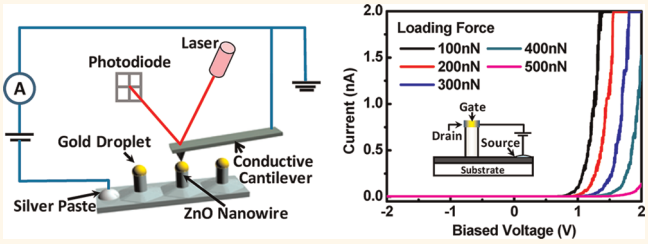
ABSTRACT



Strain-gated piezotronic transistors have been fabricated using vertically aligned ZnO nanowires (NWs), which were grown on GaN/sapphire substrates using a vapor—liquid—solid process. The gate electrode of the transistor is replaced by the internal crystal potential generated by strain, and the control over the transported current is at the interface between the nanowire and the top or bottom electrode. The current—voltage characteristics of the devices were studied using conductive atomic force microscopy, and the results show that the current flowing through the ZnO NWs can be tuned/gated by the mechanical force applied to the NWs. This phenomenon was attributed to the piezoelectric tuning of the Schottky barrier at the Au—ZnO junction, known as the piezotronic effect. Our study demonstrates the possibility of using Au droplet capped ZnO NWs as a transistor array for mapping local strain. More importantly, our design gives the possibility of fabricating an array of transistors using individual vertical nanowires that can be controlled independently by applying mechanical force/pressure over the top. Such a structure is likely to have important applications in high-resolution mapping of strain/force/pressure.

KEYWORDS: ZnO nanowire · Schottky barrier · piezotronic effect · strain-gated piezotronic transistor

As device dimensions shrink to the nanometer scale, fundamental physical limits and economic issues are likely to hinder their further scaling.[1−3] At this scale, traditional planar transistors suffer from short-channel effects and poor subthreshold characteristics.[2−5] New strategies, including the use of novel materials, innovative device architectures, and smart integration schemes, need to be explored.[2,6,7] One concept is to fabricate vertical nanoscale transistor arrays in three dimensions.[6,8,9] Such an arrayed structure provides an attractive approach to achieve high-density assembly.[10] Unfortunately, in surround-gate or wrap-around-gate field effect transistor (FET) arrays,[7,8] all elements share the same gate and cannot work independently, which may limit their further applications.

Recent research on piezoelectric transistors based on lateral single ZnO nano/microwires[11−17] demonstrates the possibility of fabricating vertical transistors gated by external strain. A piezotronic transistor is an electronic device that operates on the basis of an applied force/pressure to control the Schottky barrier (SB) and hence the charge transport characteristics, known as the piezotronic effect.[11,13,18] A typical piezotronic transistor is a metal—nanowire—metal structure,[11,13] whose gate signal is a mechanical force that can be applied on either end of the nanowire (NW). If we fabricate such devices into an array using aligned NWs, by applying a spatially varying strain on the top of the NWs, it is possible to allow each element to have its own independent "gate voltage"; thus, each of them may work independently and the whole as a transistor array. It could also be considered as a force sensor array that converts mechanical signals into electrical signals for mechanical action recording or human—machine communication.[13]

Previous reports mainly concentrated on the fundamental principles of piezotronic effect based on reversely biased Schottky junctions using lateral piezoelectric micro/nanowires bonded by two metal electrodes at the ends.[14−16] In such a metal—nanowire—metal structure, a piezotronic effect occurs at both ends of the NW by changing the local contacts with piezopotential when

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external stress is applied.[13,17] In a typical n-type ZnO piezoeletric transistor, the negative piezopotential side raises the barrier height, while the positive piezopotential side lowers the barrier height owing to the polarity of the piezopotential.[13,17] The electrical characteristics are dominated by the reversely biased Schottky junction due to the higher voltage drop across the reversely biased junction compared to the forward biased junction when connected in series.[16] The observed phenomenon is a coupling of two back-to-back Schottky junctions. However, it is important for transistors that can work under both forward and reverse bias to fulfill different applications, such as reversely biased transistors for photodetectors and forward biased transistors as light-emitting diodes.[19]

In this paper, we demonstrate strain-gated piezotronic transistor arrays using vertically aligned ZnO NWs. Each ZnO NW with an Au droplet on the tip serves as a transistor. The stress-sensitive gate is the Au–ZnO Schottky junction at the NW tip, and the other side is an Ag–ZnO junction. The piezotronic effect was observed in both forward and reversely biased piezoeletric transistors. The electrical transport characteristics of the transistors were investigated by conductive atomic force microscopy (AFM) in contact mode under different strains. Stable and repeatable current–voltage (I–V) characteristics were observed in our experiment. The current flowing through the NWs was successfully tuned/gated by external force applied to the NWs.

RESULTS AND DISCUSSION

The ZnO NWs were epitaxially grown on GaN thin films supported by sapphire substrates using Au nanoparticle catalysts, which were located at the tips of the NWs and served as the electrical contacts after the NWs' formation. To guarantee the measured electrical behavior is from a single isolated NW, we selected NWs with low aspect ratios and low density for measurements.

Reverse Mode. There are two junctions in the piezoelectric transistor in this paper: Au–ZnO and Ag–ZnO. When a bias voltage is applied, one junction is forward biased, while the other one is reversely biased. If the Schottky junction Au–ZnO is reversely biased, the Au droplet is connected to the negative voltage and the Ag paste electrode is connected to the positive. In this mode, the dominant piezotronic effect on the I–V characteristics is from the Au–ZnO junction due to the higher consumption of the voltage across this junction compared to the forward biased.[16]

Figure 1a and b show the scanning electron microscopy (SEM) images of the ZnO NWs in the device for reverse mode measurements. Each bright spot in Figure 1a corresponds to a vertical ZnO NW with a gold catalyst droplet on the tip. The average spacing

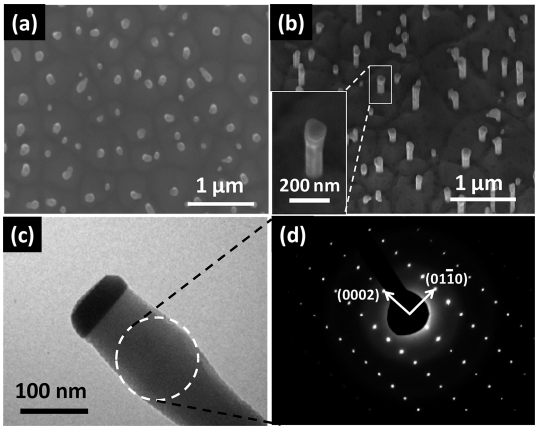

Figure 1. ZnO nanowires used for the reverse mode sample that were grown *via* a vapor–liquid–solid (VLS) deposition on a GaN epilayer: (a) top-down SEM image view; (b) SEM image at a tilt angle of 30° and a higher magnification image of a single nanowire (inset); (c) typical TEM image of a single ZnO NW with a gold droplet on its tip; (d) selected-area electron diffraction pattern from the region indicated by a dashed circle in image (c).

between two adjacent NWs is about 250 nm, and the diameter of the NWs is about 80–180 nm (Figure 1b). All of the NWs are vertically arranged on the surface, although the diameter and length may vary. Figure 1c is a transmission electron microscopy (TEM) image of a typical single NW with a diameter of ~100 nm. A distinct boundary between the Au catalyst droplet and the ZnO NW can be observed. Figure 1d gives a selected area electron diffraction (SAED) pattern of the dashed circle area in Figure 1c. This is a more effective evidence of the *c*-axis-oriented and epitaxial growth of the ZnO NWs by the vapor–liquid–solid (VLS) method using Au as catalyst as reported elsewhere.[20,21]

The I–V characteristics of the transistors were examined by conductive AFM. Figure 2a gives a schematic diagram of this measurement setup. A conductive AFM probe was used to perform nanometric contact on the transistors. The AFM probe was grounded, and the bias voltage was applied from the bottom of the sample stage. The structure of the piezoelectric transistor is Ag–ZnO–Au, and the Ag–ZnO junction is stress-free. One electrode is Ag paste coated on the as-formed ZnO conductive layer, which serves as the source, and the other electrode is the gold droplet formed at the tip of the NW, which serves as the drain. The "gate voltage" was created from the piezoelectric potential in the NW by applying an axial force using the AFM probe. The current through the NW was collected and measured using the conductive AFM system. During the electrical measurements, various compressive forces were applied to the NWs by adjusting the deflection voltage of the cantilever that had a linear relationship to the magnitude of the contact force between the AFM tip and the samples.

Strain-dependent I–V characteristics have been observed in the ZnO NW transistors. Typical rectifying

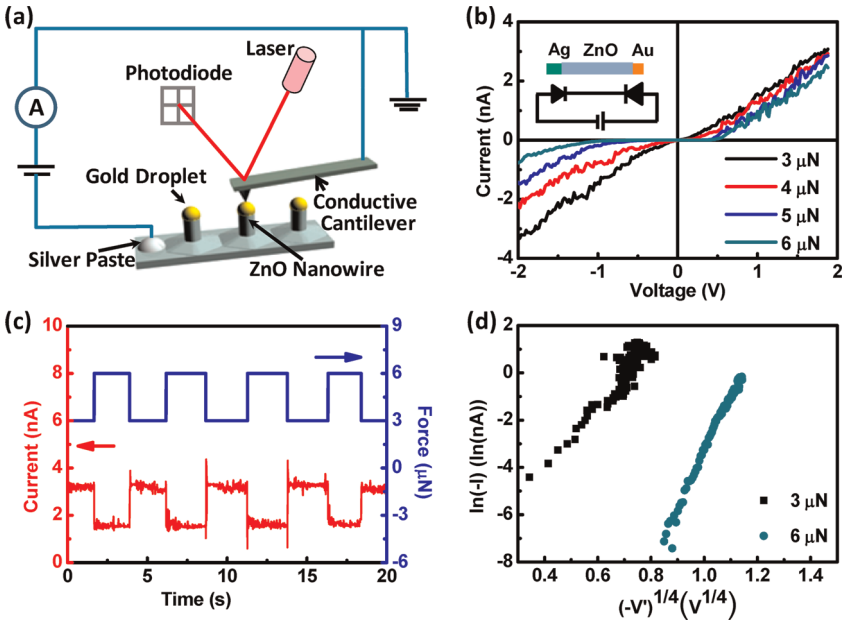

Figure 2. (a) Schematic of the conductive AFM system used for nanoscale positioning and electrical measurement; (b) typical $I-V$ characteristics under various compressive forces of a sample with double-Schottky junctions; (c) current response to a force pulse from 3 to 6 μN; the blue line is the applied force and the red is the resulting current; (d) plots of ln($-I$) as a function of $(-V)^{1/4}$, by using the data from the negative biased region in part (b).

behavior under different forces of a transistor is presented in Figure 2b. After overcoming the influence of the contact resistance between the AFM tip and the gold droplet, a force from 3 to 6 μN was applied to the transistor. As shown in Figure 2b, the current decreased when the magnitude of the compressive force increased. At a lower strain with a force of 3 μN, the $I-V$ characteristic is symmetric and close to linear (black line in Figure 2b). By increasing the applied force, the shape of the $I-V$ curves changed from symmetric to asymmetric and turned into a single Schottky-diode-like characteristic when the force was increased up to 6 μN. The current flowing through the NW has been tuned by the intensity of the external force.

The current response to periodic force pulses was also measured at constant biases. Figure 2c illustrates the dynamic response to a force pulse at a bias of -2 V. The blue line shows the applied force on the transistor alternating between 3 and 6 μN, and the red line is the response signal of current. This shows that the effect of force on the current is reversible. At a fixed bias of -2 V, the current dropped from 3.6 nA to 0.5 nA after applying a 6 μN force on the NW, which can be considered as the "on" and "off" states in a switch transistor. The on$-$off ratio is about 7.2, which can be further tuned by increasing the strain.

The inset in Figure 2b shows the device structure and an equivalent circuit of the transistor. The transistor can be equivalent to two back-to-back Schottky junctions. For back-to-back Schottky junctions, the voltage is mainly consumed at the reversely biased SB.[16] The voltage dependence of the reverse current flowing through a SB is mainly due to the image-force-induced barrier height lowering.[19] When an electron was injected from the metal electrode into the semiconductor, it induces a positive charge at the interface layer, which acts like an image charge within the layer. The conduction band bends downward and the valence band bends upward, respectively. This effect leads to a reduction of the SBH. The dependence of the reverse current I_r on the reverse bias follows the equation[16,19]

$$I_r = AA^{**}T^2 \exp\left(-\frac{\varphi_B}{k_B T}\right) \exp\left(\frac{q\sqrt{\frac{q\xi}{4\pi\varepsilon_s}}}{k_B T}\right) \quad (1)$$

where A is the area of the Schottky contact, A^{**} is the effective Richardson constant, T is the absolute temperature, ϕ_B is the Schottky barrier height (SBH), k_B is the Boltzmann constant, q is the electron charge, and

$$\xi = \sqrt{\frac{2qN_D}{\varepsilon_s}\left(V_r + V_{bi} - \frac{k_B T}{q}\right)} \quad (2)$$

N_D is the donor density, ε_s is the dielectric constant of the semiconductor, and V_{bi} is the built-in potential at the barrier. Under the condition of $V_r \gg V_{bi}$ and $(k_B T)/q$, the dependence of I_r on V_r can be written as

$$\ln I_r \propto V_r^{1/4} \quad (3)$$

To verify that the model can be used to describe the observed phenomenon, the curves of ln($-I$) as a function of $(-V)^{1/4}$ using the data from Figure 2b ($V < 0$) were plotted in Figure 2d. Under two typical strains, 3 and 6 μN, both plots show a good linear relationship, as expected. It is reasonable to expect that the

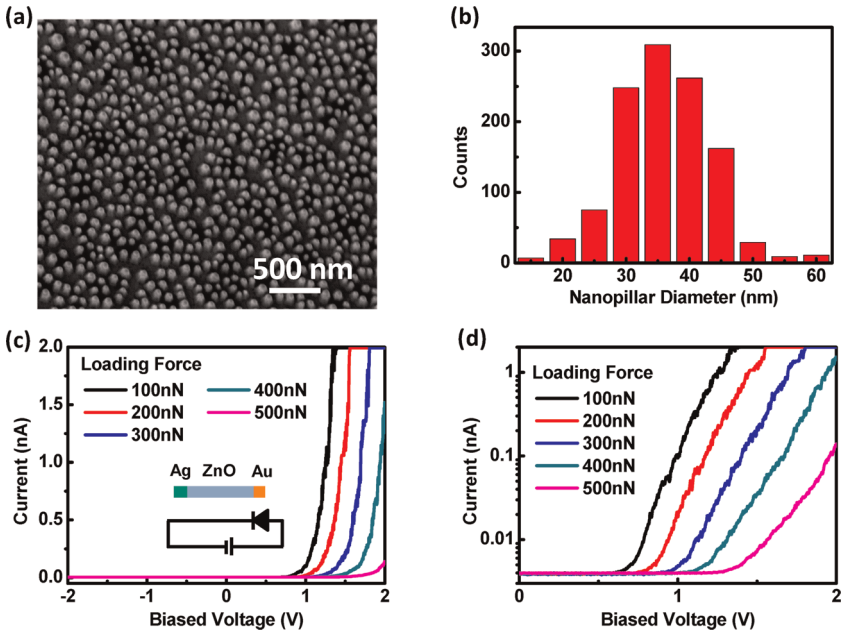

Figure 3. (a) ZnO nanowires used for the forward mode sample; (b) diameter distribution of the nanowires; (c) *I*–*V* characteristics under various compressive forces of a sample with single-Schottky junctions; (d) current–voltage characteristics plotted on a semilogarithmic scale.

transportation behavior at the reversely biased side is dominated by the reversely biased SB.

Forward Mode. In forward mode, the piezo Schottky junction (Au–ZnO) is forward biased. A positive voltage is applied between the Au droplet and the Ag paste. In this mode, the Ag–ZnO junction is reversely biased, and it will consume most of the voltage if the barrier is high. To eliminate this effect, a device with a lower barrier height at the Ag–ZnO junction was obtained by annealing the device at 600 K in ambient atmosphere for 12 h. Figure 3a shows the SEM image (30°-tilted view) of ZnO NWs for a typical device. It is apparent that the NWs are short. The ZnO NWs used in this device are more like small nanopillars with a diameter of around 35 nm. Figure 3b shows a distribution of the NW diameters as determined from a non-tilted SEM image.

The *I*–*V* characteristics of the device under various strains are shown in Figure 3c. Under negative voltage, only a small amount of current can go through. Under positive voltage, the current can reach several nanoamperes. When the external stress varies from 100 to 500 nN, there is a sharp decrease in the current. The device performs like a single Schottky diode. This indicates that the Schottky barrier formed at the Au–ZnO junction is high and dominates the performance of the device. The inset in Figure 3c shows the device structure and an equivalent circuit.

For an ideal Schottky diode, the *I*–*V* characteristics in the forward direction are described by[19]

$$I_f = AA^{**}T^2 \exp\left(-\frac{\varphi_B}{k_B T}\right) \exp\left(\frac{qV_f}{nk_B T} - 1\right) \quad (4)$$

where V_f is the voltage dropped on the forward biased Schokkty diode and n is the ideality factor.[19] Mathematically, the logarithm of the current ($\ln I_f$) has a linear relationship to the voltage (V_f) dropped on the diode and can be expressed as

$$\ln I_f \propto V_f^{1/4} \quad (5)$$

Figure 3d shows the forward *I*–*V* characteristics of this transistor on a semilog scale. The good linear fit of the plots shows that the forward current has an exponential relationship to the voltage. This indicates that the thermionic emission–diffusion model is the dominant process in our device.

The stress-dependent *I*–*V* characteristics, in both forward and reverse modes, can be explained by the piezotronic effect. Figure 4a and b show the mechanism of the piezotronic effect in ZnO NWs.[13] ZnO has a noncentral symmetric wurtzite crystal structure (Figure 4a). Zn^{2+} cations and O^{2-} anions are tetrahedrally coordinated, and the centers of the positive ions and negatives ions overlap with each other. When a stress is applied at the apex of the tetrahedron, the charge centers are relatively displaced, resulting in a dipole moment. A piezoelectric field is created by adding up all the dipoles, and there would be a macroscopic potential drop along the straining direction in the crystal. When a compressive strain is applied to the piezoelectric ZnO NW along the *c*-axis, a piezopotential field is generated in the NW. For the sake of simplicity, we calculated the potential distribution using the finite element method by assuming the ZnO NW as an insulator. The color code plotted in Figure 4b shows the calculated potential distribution

along the *c*-axis-oriented ZnO NW while various compressive strains are applied along the NW (0, 100, and 200 nN from left to right). The NW dimensions of the NW are 50 nm in diameter and 100 nm in length. The calculated piezopotential is based on the following parameters: piezo constant $d_{33} = -5.43 \times 10^{-12} C/N$, relative dielectric permittivity $\varepsilon_r = 10.204$, and the elasticity is 210 GPa, which are the default parameters for piezoelectric ZnO materials in the COMSOL Multiphysics software (Version 4.2a), and there is no doping. The dependency rate of the piezopotential on the stress is about 5 mV/nN, as shown in Figure 3b. In nanowires that are n-type doped or containing vacancies, the piezopotential will drive the free electrons to move from one side to the other side to "screen" the local piezopotential in the crystal and reach a new equilibrium. Due to the finite doping of the ZnO NWs, the piezopotential is partially screened but not completely, and the partially screened piezopotential will change the local Fermi level and conduction band near the surface. The piezopotential affects the SBH by changing the local Fermi level and conduction band at the semiconductor side of the Schottky junction.[13] In our case, the ZnO NW is capped by an Au droplet and the bottom is connected to the as-grown ZnO conductive layer. The piezotronic effect mainly influences the Au–ZnO Schottky junction.

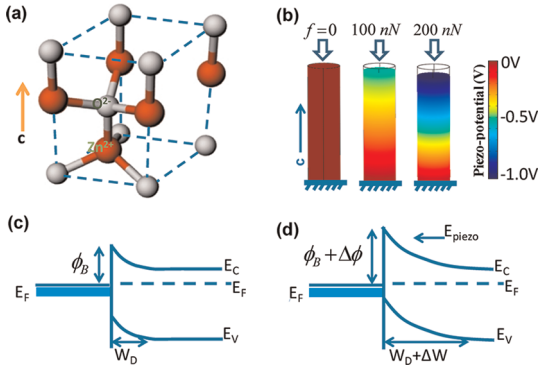

Figure 4. (a) Ball-and-stick representation of the ZnO wurtzite crystal structure. Red and gray spheres denote Zn and O atoms, respectively. (b) Finite element calculation of the piezopotential distribution in a ZnO nanowire ($d_{33} = -5.43 \times 10^{-12} C/N$, $\varepsilon_r = 10$) 50 nm in width and 100 nm in length, under different uniaxial compressions of 0 nN (left), 100 nN (middle), and 200 nN (right). (c) Schottky barrier formed at the metal–semiconductor interface. (d) Piezopotential influence on the Schottky barrier height at the metal–semiconductor junction on the (0001) plane.

To illustrate the piezotronic effect simply, we can use the energy band diagrams shown in Figure 4c and d. The barrier height ϕ_B is quantitatively evaluated by the potential difference between the Fermi energy of the metal and the band edge of the n-type semiconductor where the electrons reside as shown in Figure 4c. If the semiconductor is a piezoelectric material, ZnO for example, and the crystallographic *c*-axis is directed toward the Au–ZnO junction, a piezopotential would be created in the crystal once a strain is applied as depicted in Figure 4d. The local contact characteristics are changed by the piezopotential due to the redistribution of the carriers. The *c*-axis of the vertical ZnO NWs grown on GaN-buffered *c*-plane sapphire is along the growth direction. When an external force is applied, there is a negative piezopotential generated at the Schottky junction between the Au droplet and the ZnO NW, which widens the depletion layer as shown in Figure 4d, thus enhancing the SBH. The strain-dependent piezopotential effectively changes the local contact characteristics and tunes/gates the carrier transport process at the metal–semiconductor interface.

Furthermore, we studied the piezoeletric transistors based on the ZnO NWs varied from 20 to 200 nm in diameter and 60 to 600 nm in length. We have calculated the barrier height increment according to the ln *I*–*V* plot.[16,19] Due to the dominate contribution of the normal force on the piezotronic effect,[22,23] we have neglected the bending effect and assumed that the force is applied along the axis of the vertical NWs. The results show that all of the barrier heights increase with compressive strain, just as expected for NWs growing along the +*c*-axis. Figure 5a and b show typical relationships between the increment of SBH and the strain with different lengths. This indicates that the piezotronic effect occurs at the Schottky junction, which is consistent with previous theoretical reports.[11]

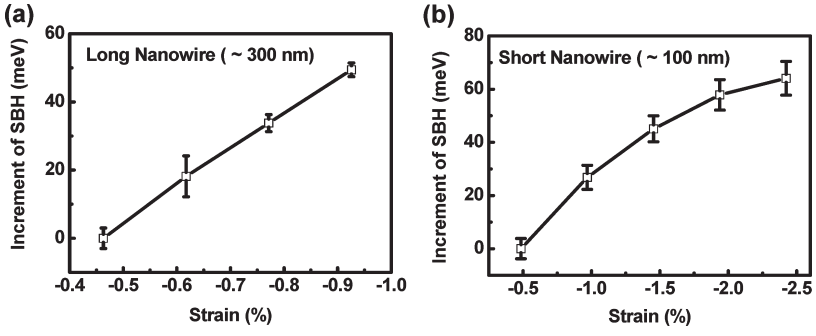

Figure 5. Schottky barrier increment with the strain at the Au–ZnO junction of a long nanowire device of ~300 nm (a) and a short nanowire device of ~100 nm and (b) calculated according to a thermionic emission–diffusion model.

Piezoresistance also contributes to the observed effect, barrier height, and sensitivity, but the dominant effect in our devices is still the piezotronic effect. The piezotronic effect is a coupling between the piezoelectric effect of the material and its semiconductor properties and functionalities.[13,17] ZnO is a material that simultaneously has semiconducting and piezoelectric properties.[18] The piezoresistive effect describes the change in resistivity of a semiconductor due to applied mechanical stress because of the change in band gap, charge carrier density, and possibly the decreased mobility as a result of the strained lattice. The piezoresistive effect differs from the piezotronic effect in that the piezoresistive effect causes a change only in electrical resistance without polarity, and it is mainly dominated by the volume and surface area of the NW. The piezotronic effect is about the same as the nonsymmetric effect of the piezopotenital on the two end contacts, which selectively acts on one side of the metal–semiconductor contact/interface due to the polarity of the piezopotential.[16] The nonsymmetric behavior observed in our experiment is mainly due to the piezotronic effect.

CONCLUSIONS

Vertically aligned ZnO NWs capped with Au droplets were used as a piezoeletric transistor array. Each NW serves as a single transistor. Ag paste coated on the as-formed ZnO conductive layer serves as the source, and Au droplets at the tips of the NWs serve as the drains. The drain–source voltage was applied through a conductive AFM, and the "gate" voltage is the inner crystal piezoelectric potential created along the NWs by the stress applied using the AFM probe. The I–V characteristics were investigated under both reverse and forward working mode. The current flowing through the piezoeletric transistors was successfully tuned/gated by the external force. The working principle of the transistor is governed by the piezotronic effect, which is based on the tuning of the local SB by the piezopotential. Our study demonstrates the first strain-gated piezoelectric transistor using vertically aligned ZnO NWs.

In the strain-gated piezotronic transistor demonstrated here, the gate electrode of the transistor is replaced by the internal crystal potential generated by strain, and the control over the transported current is at the interface between the nanowire and the top or bottom electrode. It gives the possibility of fabricating an array of transistors using individual vertical nanowires that can be controlled independently by the applied mechanical force/pressure over the top. Such a piezotronic transistor array is a new design of transistors and is likely to have important applications in high-resolution mapping of strain/force/pressure.

EXPERIMENTAL SECTION

Synthesis of Au-Droplet-Capped ZnO Nanowire Arrays. Well-aligned vertical ZnO NW arrays with Au droplets at their tips were synthesized using a VLS method by evaporating the mixture of ZnO (99.999% purity) and graphite (99.99% purity) powder (1:1 by mass) in a tube furnace. After being evacuated to 160 Torr with constant flowing O_2 gas (0.5 sccm) and Ar gas (49.5 sccm), the furnace was heated from room temperature to 960 °C with a heating rate of 50 °C/min. The furnace was kept at that temperature for the NWs to grow, and then the whole system was naturally cooled to room temperature. The desired NWs were grown on GaN/sapphire substrates coated with an Au catalyst layer. The size and distribution of the NWs were roughly controlled by the thickness of the catalyst layer, the local temperature near the substrates, and the duration of the growth process. The local temperature near the substrates was tuned by the position in the gradient temperature field between the middle heater and end cooler. The sample analyzed here had a catalyst layer ~2 nm thick, and the growth time varied from 30 min for long NWs to 5 min for short NWs.

Morphology and Structure Characterization. The morphological and crystallographic studies on the ZnO NW transistors were performed by a LEO 1530 FE-SEM system and a Hitachi HF2000 TEM.

Electrical Measurements with Conductive AFM. The performance of the piezoeletric transistors was characterized using a conductive AFM system (Molecular Force Probe MFP-3D from Asylum Research) with a conducting diamond-coated AFM probe, which has a spring constant of 4.42 nN/nm and an inverse optical lever sensitivity (InvOLS) of 226 nm/V. The force applied to the vertical ZnO NW transistor was estimated by multiplying the spring constant, InvOLS, and cantilever deflection (expressed as voltage). The magnitude of the force was monitored by changing the set point of deflection. First, a topography image of ZnO NW arrays was scanned at a speed of 5 μm/s using tapping mode with a deflection voltage of 600 mV. The AFM tip was repositioned on the top of the ZnO NWs by changing the relative position between the AFM tip and the sample stage driven by a piezoelectric driver. After finding the exact position of the NWs, the electrical measurements were carried out using the contact mode at room temperature in air.

Conflict of Interest: The authors declare no competing financial interest.

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